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(5 AND 13).PGPB,USPT.	6
(L5 AND L13).PGPB,USPT.	6

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*DB=PGPB, USPT: PLUR=YES: OP=OR*

L32 15 and 113

L31 15 and 112

L30 15 and 11

L29 15 and 19

L28 15 and 16

L27 14 and 113

J 26 14 and 112

L25 14 and 110

L24 14 and 19

L23 14 and 16

J 22 J2 and J13

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<u>L21</u>	l2 and l12	7	<u>L21</u>
<u>L20</u>	l2 and l10	113	<u>L20</u>
<u>L19</u>	l2 and l9	146	<u>L19</u>
<u>L18</u>	l2 and l6	226	<u>L18</u>
<u>L17</u>	l1 and l13	11	<u>L17</u>
<u>L16</u>	l1 and l12	22	<u>L16</u>
<u>L15</u>	l1 and l10	133	<u>L15</u>
<u>L14</u>	l1 and l9	228	<u>L14</u>
<u>L13</u>	(717/136-163)![CCLS]	5169	<u>L13</u>
<u>L12</u>	(711/141-143)![CCLS]	1832	<u>L12</u>
<u>L11</u>	l1 and l6	430	<u>L11</u>
<u>L10</u>	(712/230-240)[CCLS]	1943	<u>L10</u>
<u>L9</u>	(712/225-248)[CCLS]	5621	<u>L9</u>
<u>L8</u>	(712/2-300)[CCLS]	13606	<u>L8</u>
<u>L7</u>	(712/2-300)![CCLS]	13606	<u>L7</u>
<u>L6</u>	(712/2-300)[CCLS]	13606	<u>L6</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L5</u>	l3 and l1	470	<u>L5</u>
<u>L4</u>	l3 and l2	159	<u>L4</u>
<u>L3</u>	(convert\$3 or conversion\$1 or translat\$5) near15 (format\$4 or instruction\$1 or micro near1 instruction\$1 or macro near1 instruction\$1 or opcod\$3)	218588	<u>L3</u>
<u>L2</u>	L1 and branch\$3 near5 (predict\$5 or speculat\$5)	286	<u>L2</u>
<u>L1</u>	(fetch\$5 or pre near1 fetch\$5) near15 (order or sequenc\$4 or position\$1) near25 (buffer\$3 or fifo or lilo or lifo)	1472	<u>L1</u>

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IEEE JNL IEEE Journal or Magazine

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 1. **Beating in-order stalls with "flea-flicker" two-pass pipelining**

Barnes, R.D.; Sias, J.W.; Nystrom, E.M.; Patel, S.J.; Navarro, J.; Hwu, W.W.;  
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 2. **An analysis of the performance impact of wrong-path memory references on out-of-order execution processors**

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